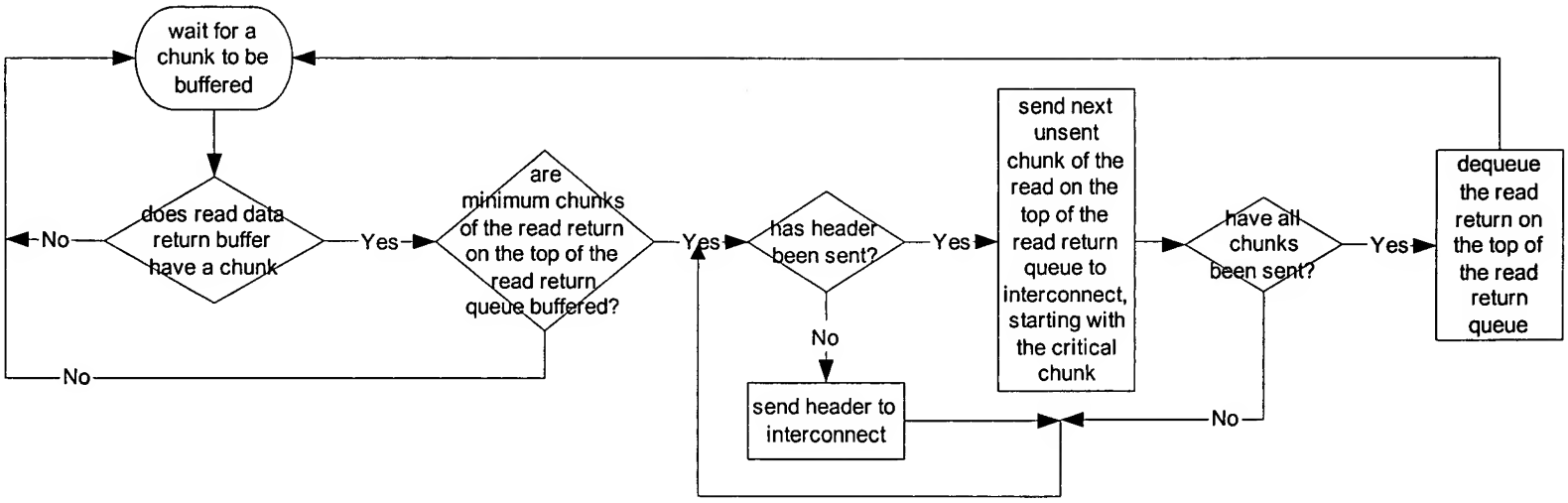
Decision in the figure may be done every flit clock cycle



Store and forward data return
Figure 1A (Prior Art)

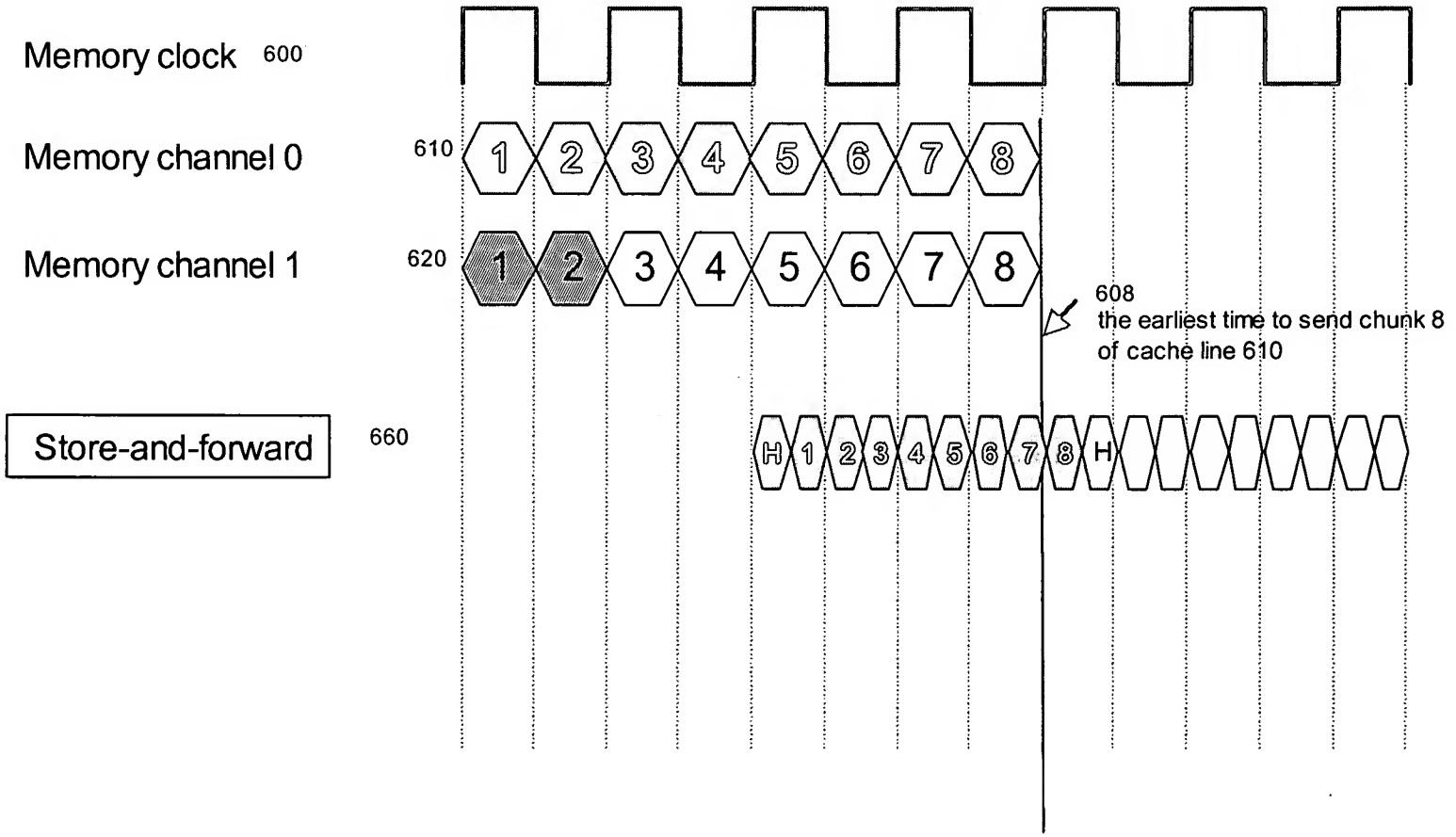

Memory clock 600
Memory channel 0
610
1 2 3 4 5 6 7 8
Memory channel 1
620
1 2 3 4 5 6 7 8
608
the earliest time to send chunk 8
of cache line 610
Store-and-forward
660
H 1 2 3 4 5 6 7 8 H

Figure 1B

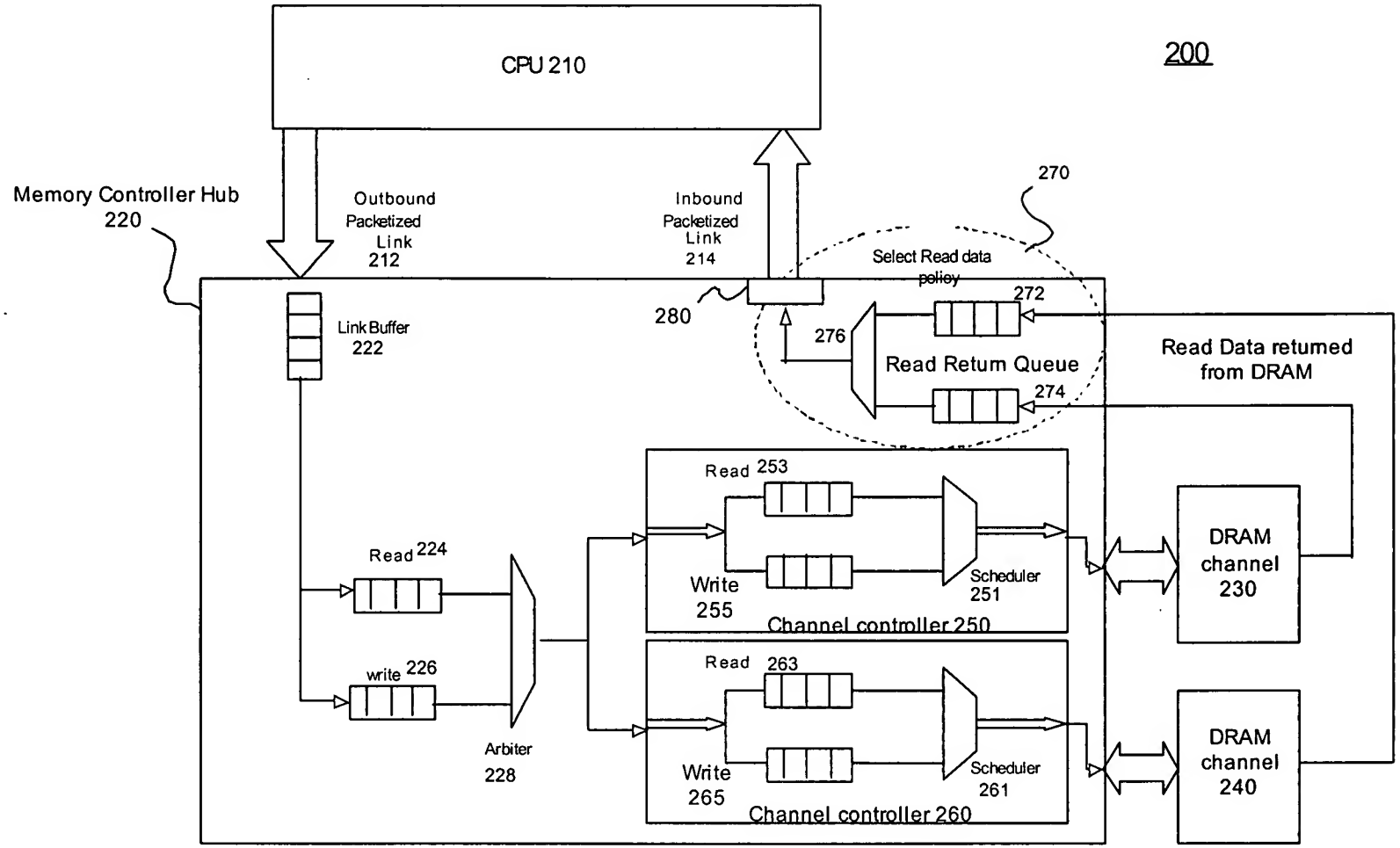
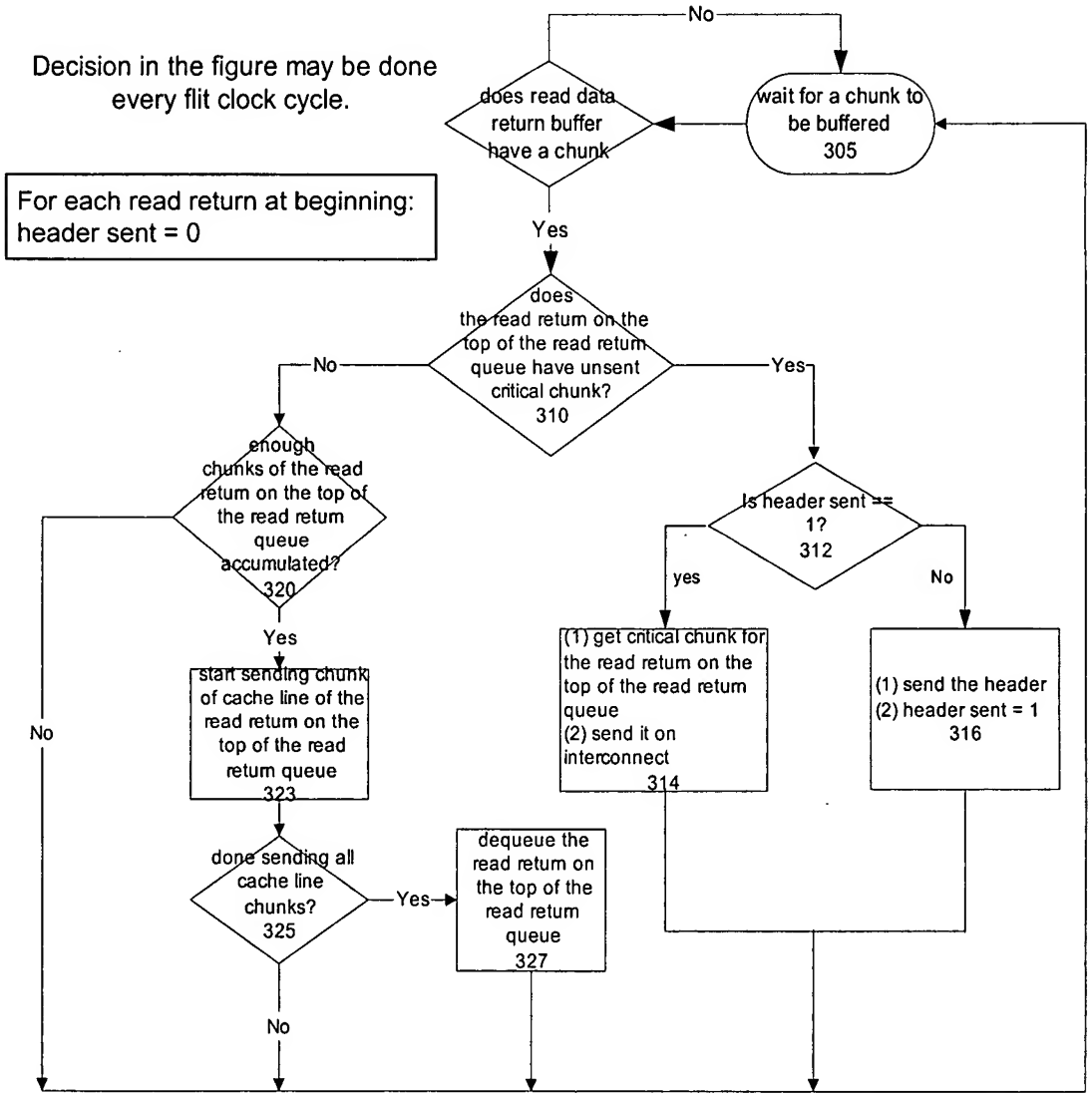

CPU 210
200
Memory Controller Hub
220
Outbound
Packetized
Link
212
Inbound
Packetized
Link
214
270
Select Read data
policy
280
272
276
Read Return Queue
274
Read Data returned
from DRAM
Link Buffer
222
Read 253
Read 224
Write
255
Scheduler
251
Channel controller 250
DRAM
channel
230
write 226
Read 263
Arbiter
228
Write
265
Scheduler
261
Channel controller 260
DRAM
channel
240

Figure 2



Critical chunk with bubble
Figure 3A

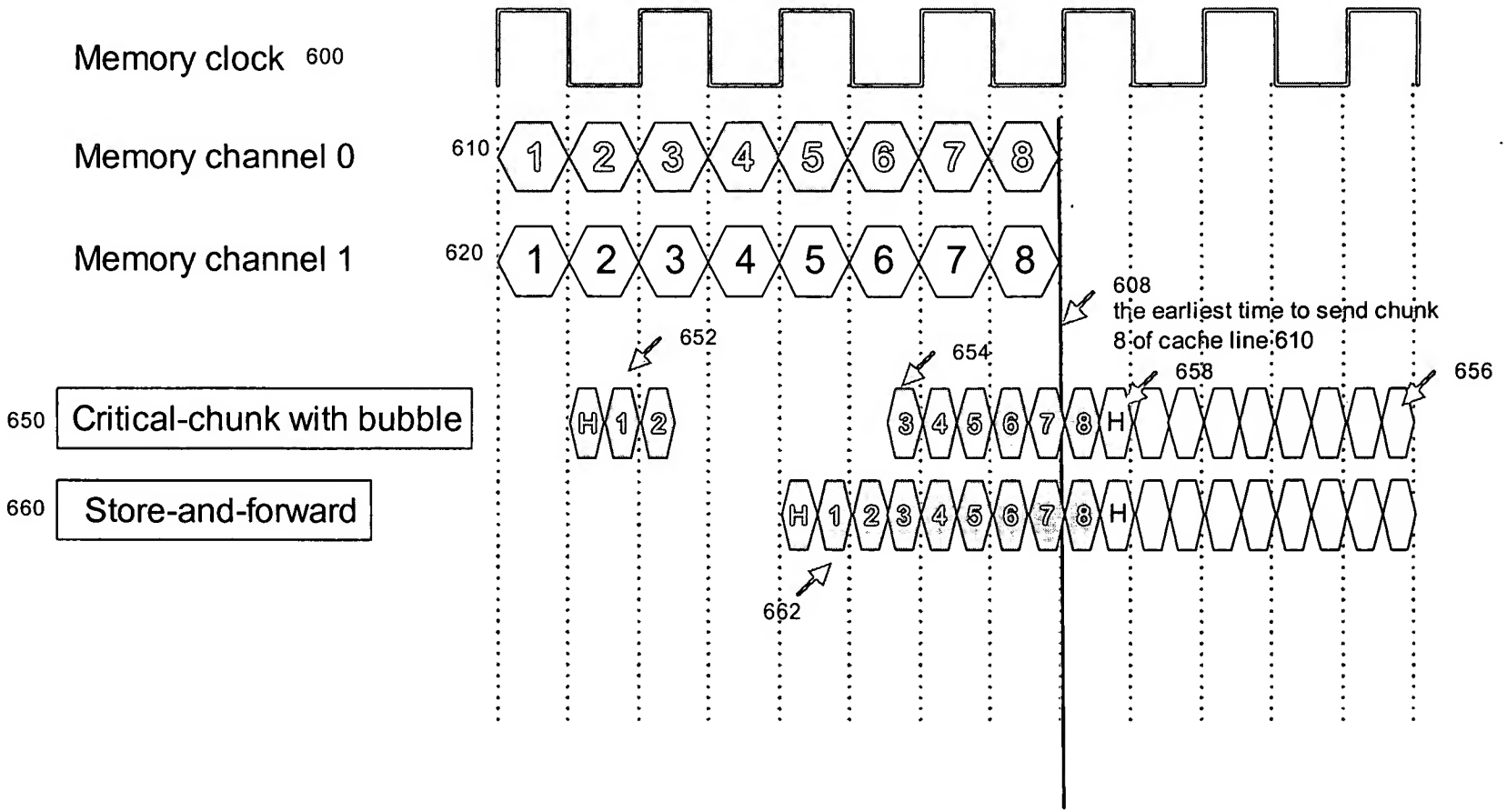
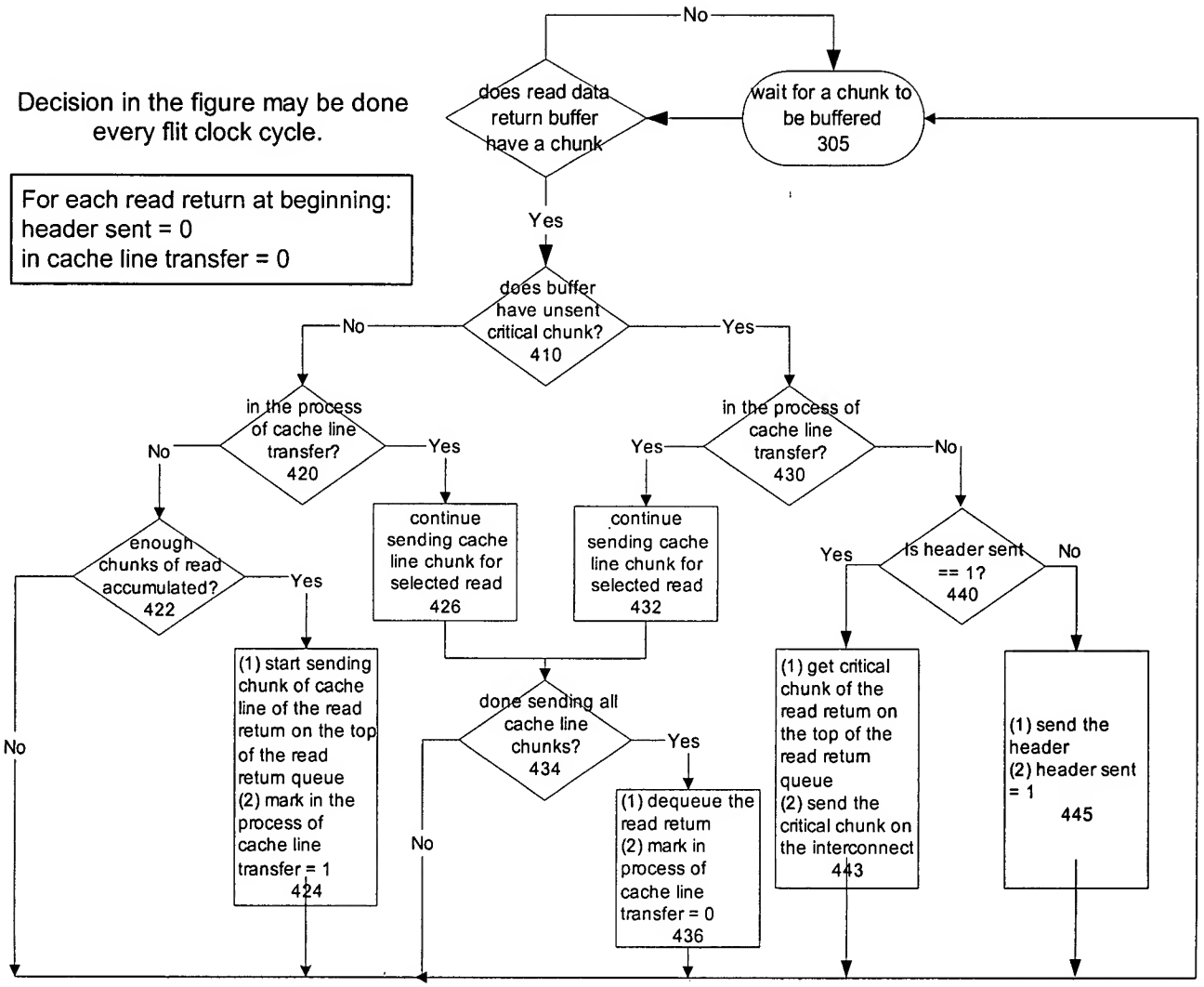

Memory clock 600
Memory channel 0
610
1 2 3 4 5 6 7 8
Memory channel 1
620
1 2 3 4 5 6 7 8
608
the earliest time to send chunk
8 of cache line 610
652
654
658
656
650 Critical-chunk with bubble
H 1 2
3 4 5 6 7 8 H
660 Store-and-forward
H 1 2 3 4 5 6 7 8 H
662

Figure 3B



Critical chunk interleaved read return
Figure 4A

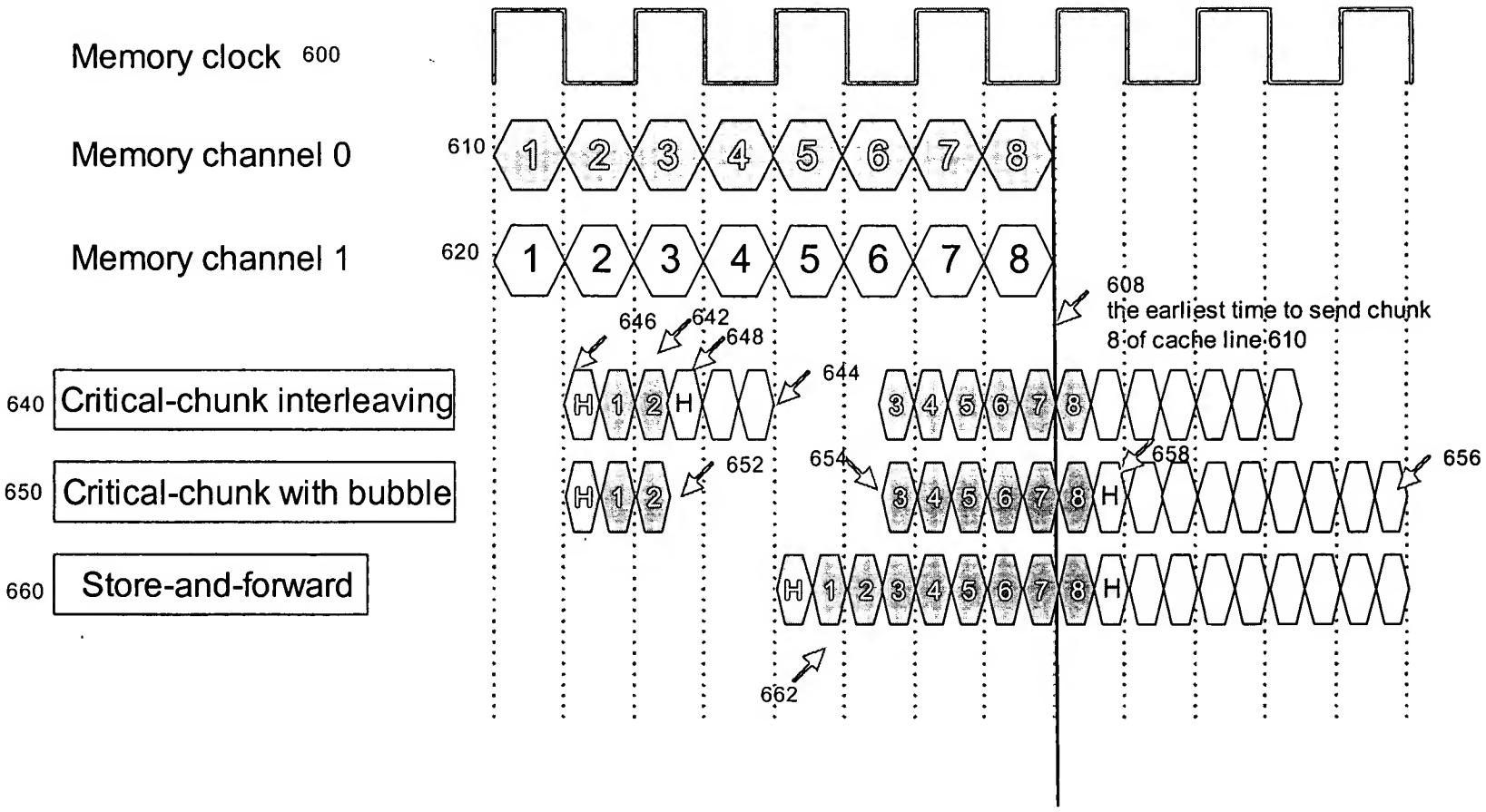
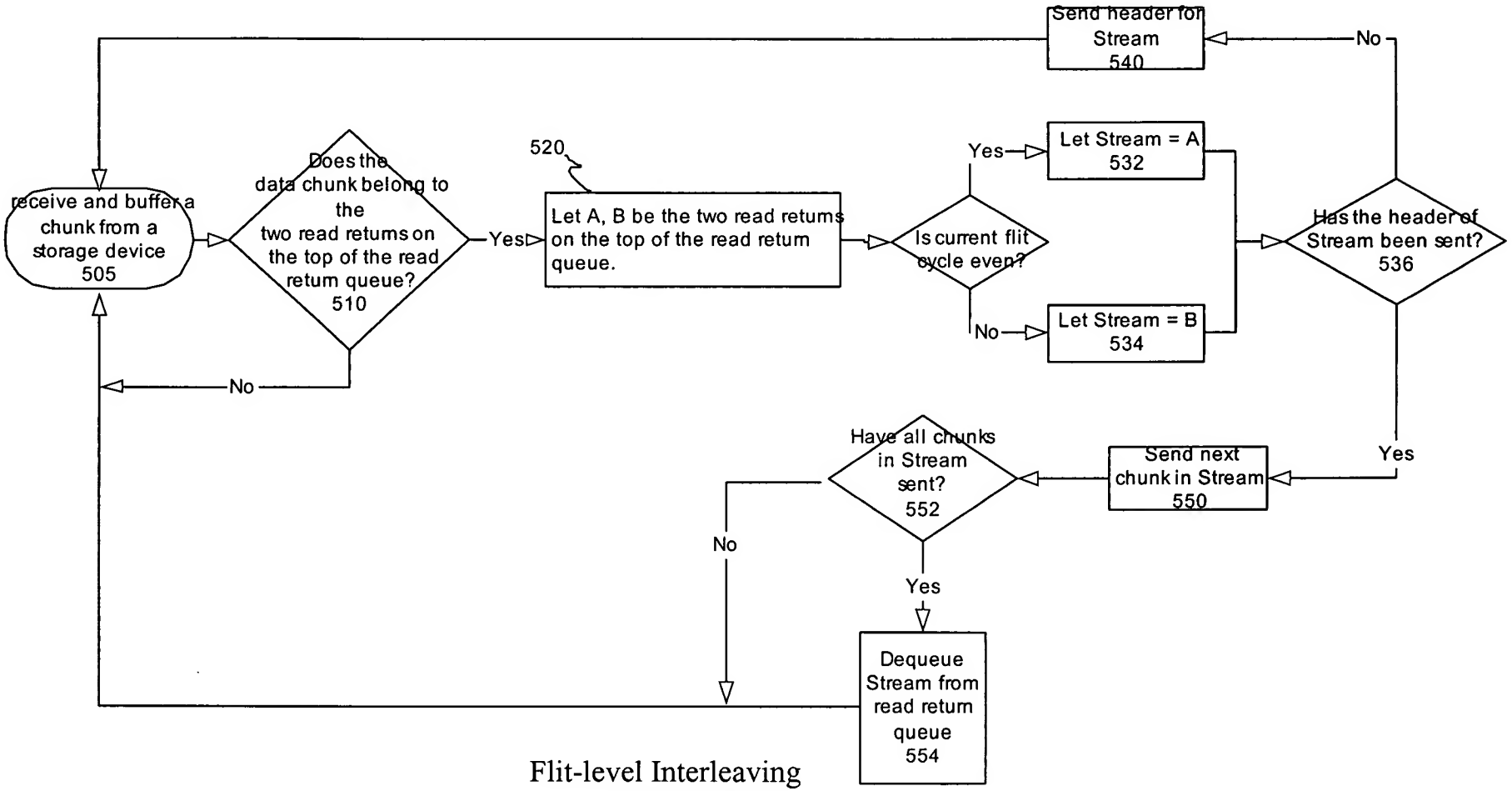

Memory clock 600
Memory channel 0
610
Memory channel 1
620
1 2 3 4 5 6 7 8
608
the earliest time to send chunk 8 of cache line 610
646
642
648
644
640 Critical-chunk interleaving
H 1 2 H
3 4 5 6 7 8
652
654
658
656
650 Critical-chunk with bubble
H 1 2
3 4 5 6 7 8 H
660 Store-and-forward
H 1 2 3 4 5 6 7 8 H
662

Figure 4B

Decision in the Figure may be done every flit clock cycle.



Flit-level Interleaving
Figure 5A

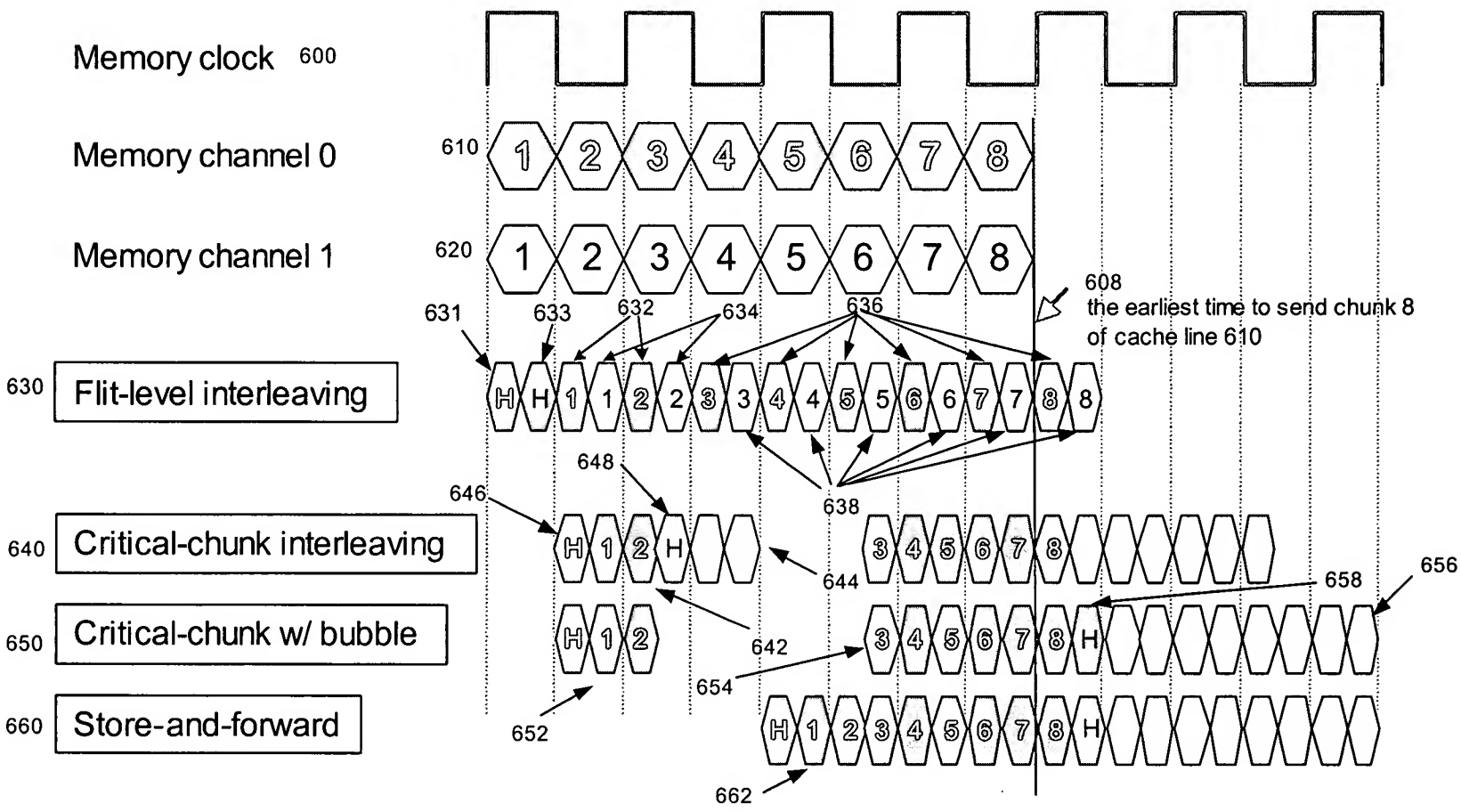

Memory clock 600
Memory channel 0
610
Memory channel 1
620
608
the earliest time to send chunk 8
of cache line 610
631
633
632
634
636
630 Flit-level interleaving
H H 1 1 2 2 3 3 4 4 5 5 6 6 7 7 8 8
648
646
638
640 Critical-chunk interleaving
H 1 2 H
3 4 5 6 7 8
644
658
656
650 Critical-chunk w/ bubble
H 1 2
642
3 4 5 6 7 8 H
654
660 Store-and-forward
652
H 1 2 3 4 5 6 7 8 H
662

Figure 5B

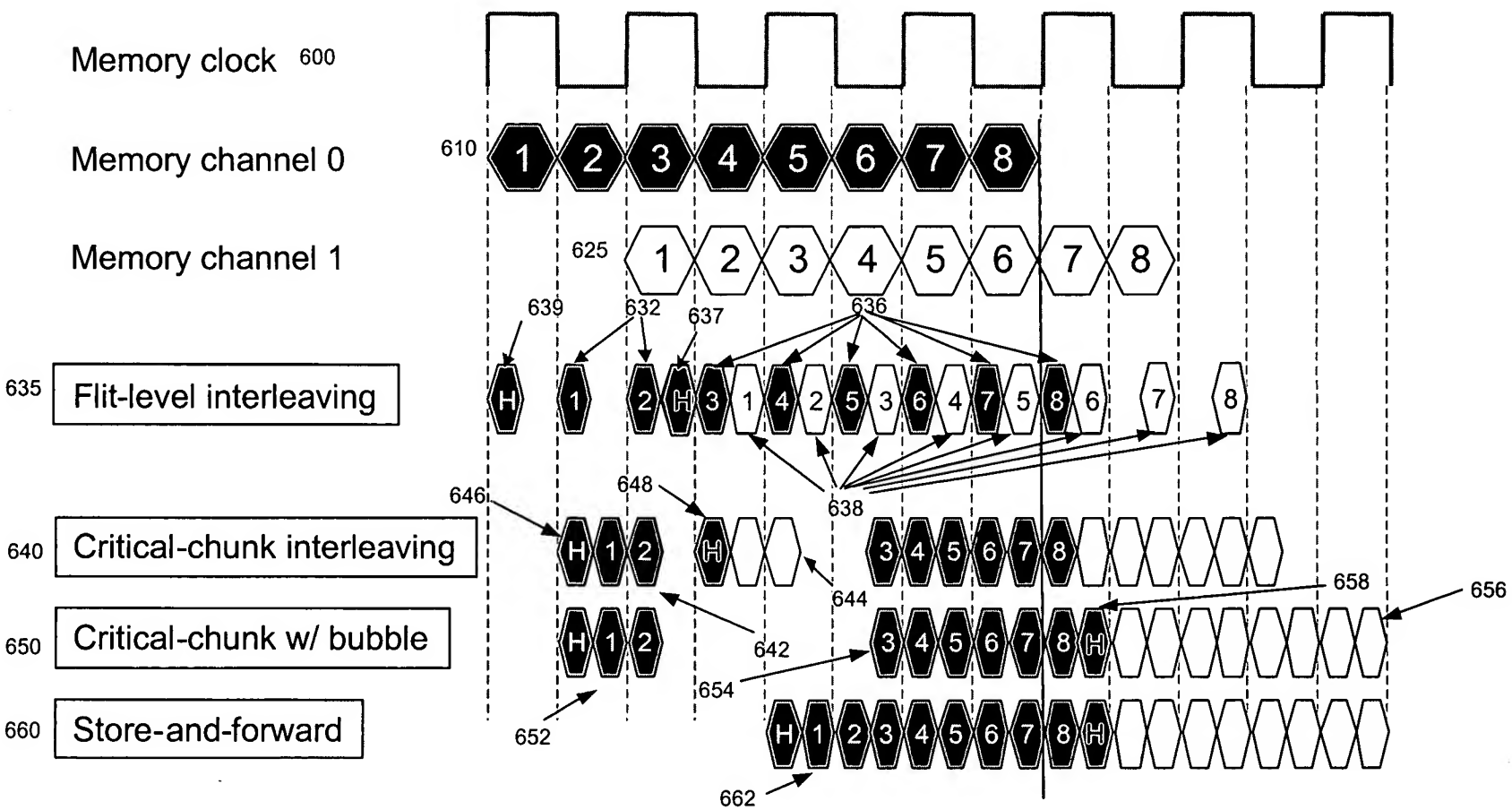

Memory clock 600
Memory channel 0
Memory channel 1
610
625
635 Flit-level interleaving
640 Critical-chunk interleaving
650 Critical-chunk w/ bubble
660 Store-and-forward
639
632
637
636
638
646
648
644
642
652
654
656
658
662

Figure 5C

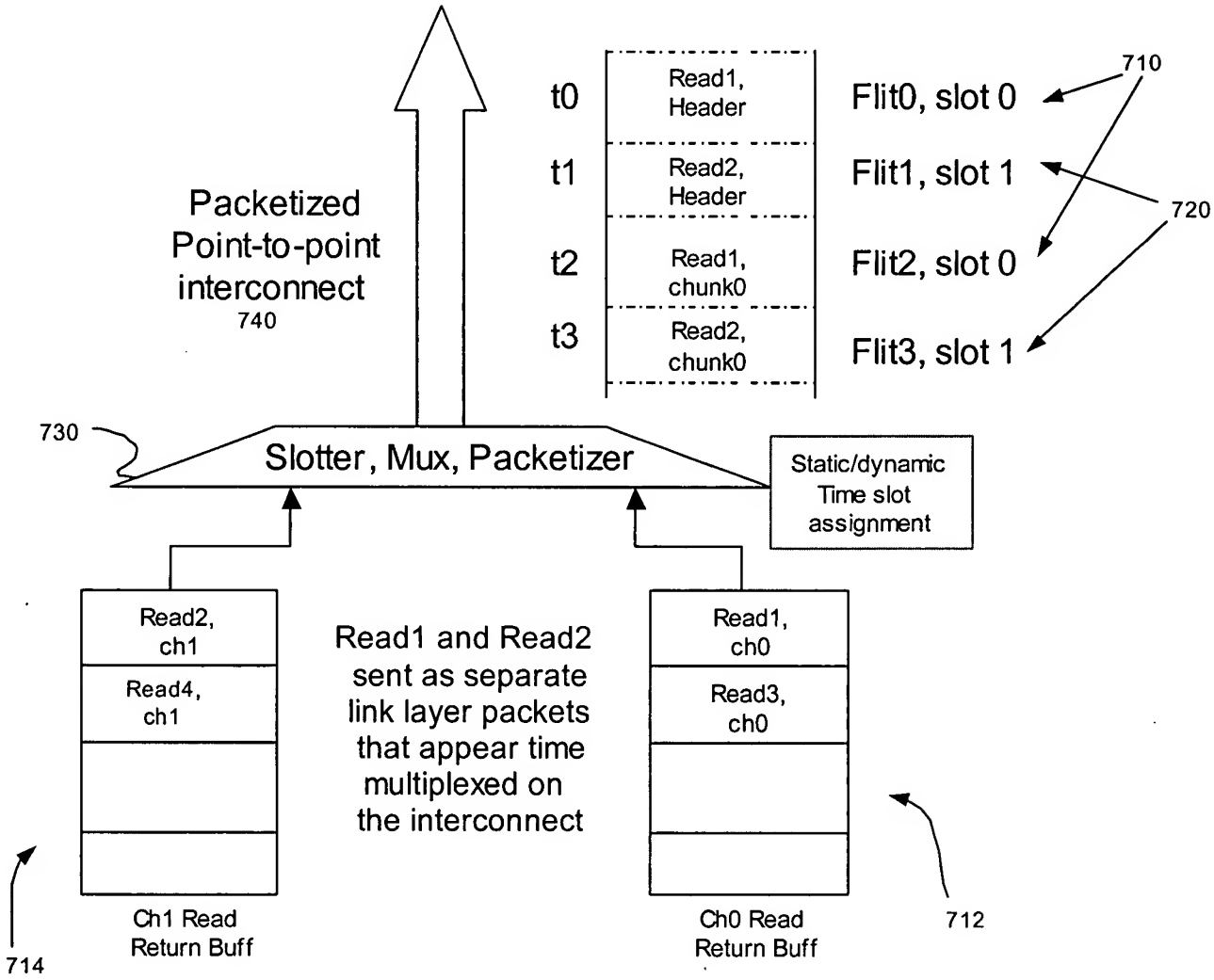
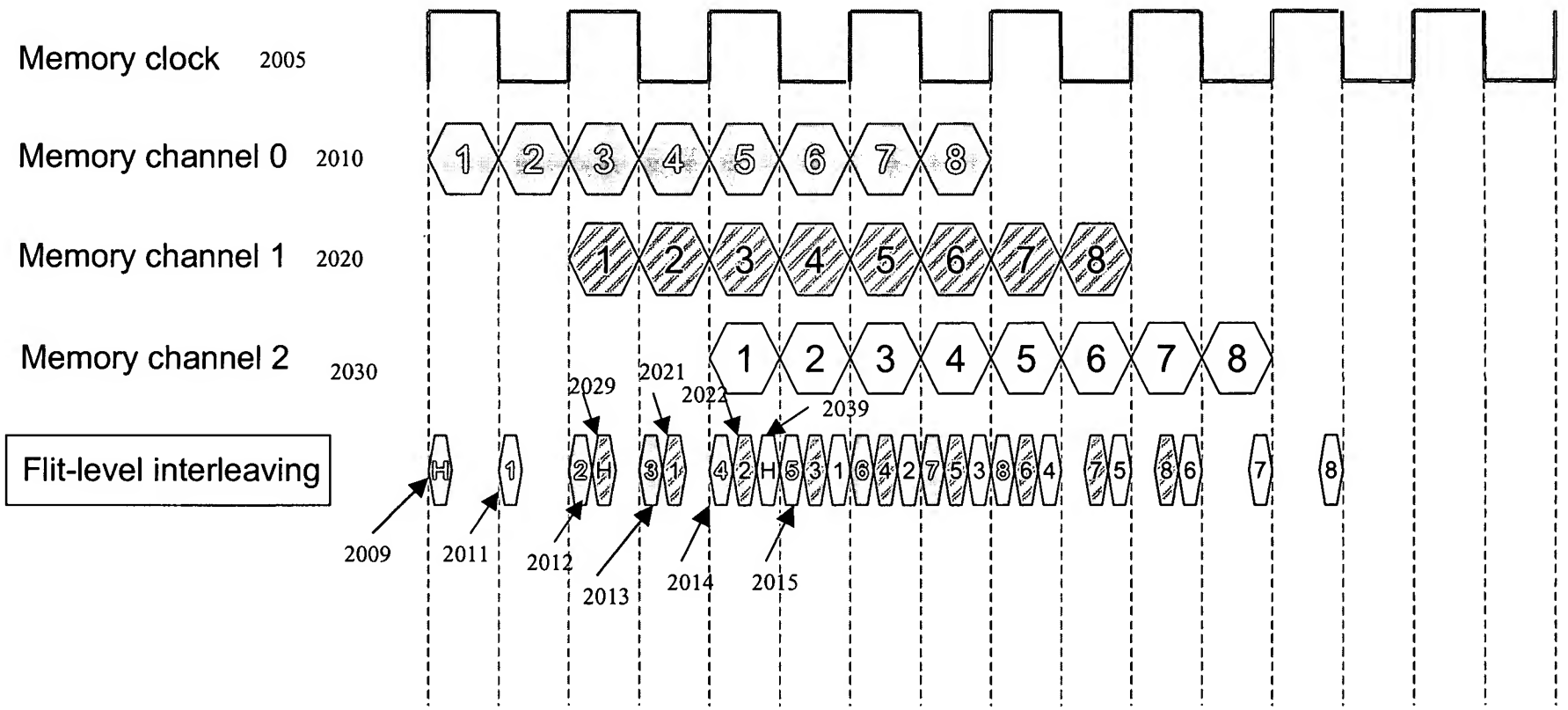
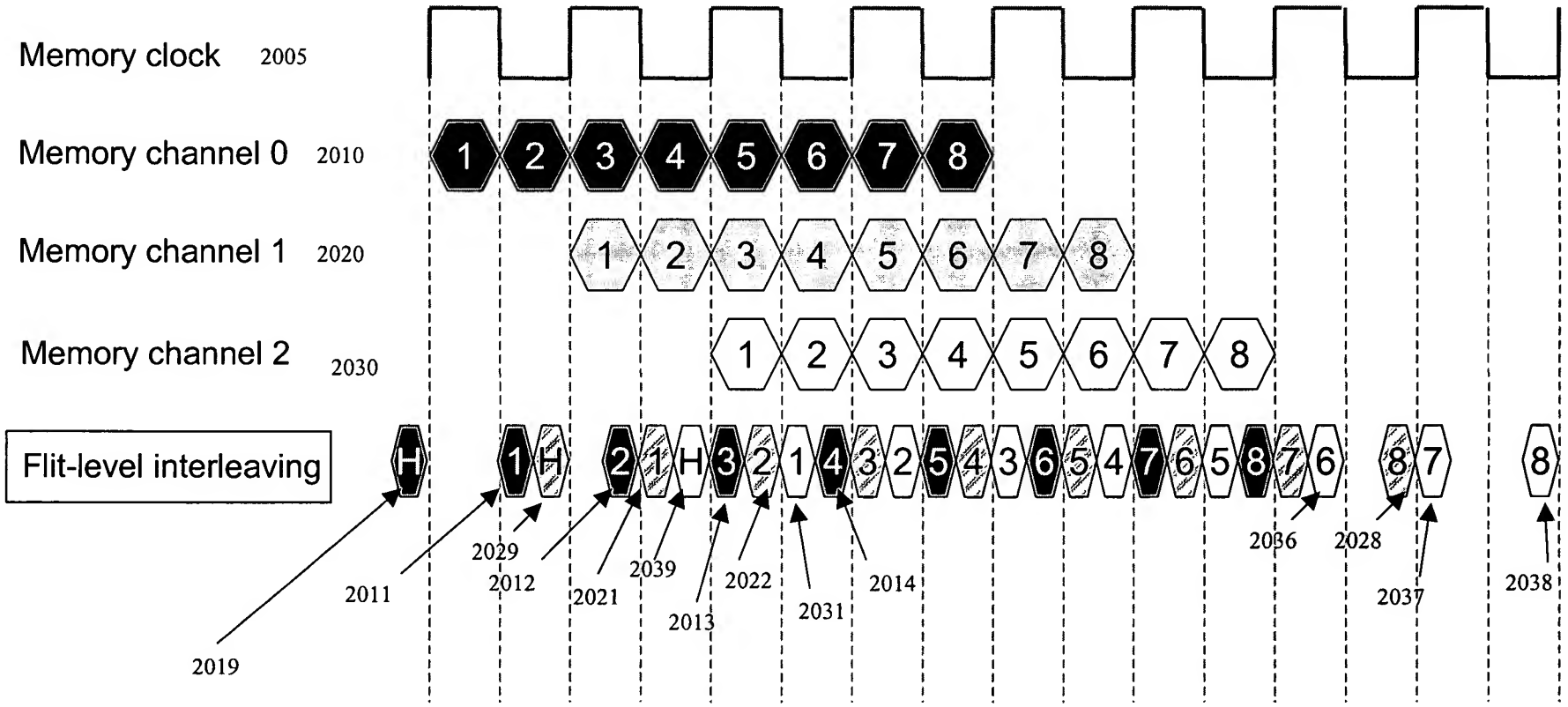

Packetized
Point-to-point
interconnect
740
t0
Read1,
Header
t1
Read2,
Header
t2
Read1,
chunk0
t3
Read2,
chunk0
Flit0, slot 0
Flit1, slot 1
Flit2, slot 0
Flit3, slot 1
710
720
730
Slotter, Mux, Packetizer
Static/dynamic
Time slot
assignment
Read2,
ch1
Read4,
ch1
Read1 and Read2
sent as separate
link layer packets
that appear time
multiplexed on
the interconnect
Read1,
ch0
Read3,
ch0
Ch1 Read
Return Buff
Ch0 Read
Return Buff
712
714

Figure 6A



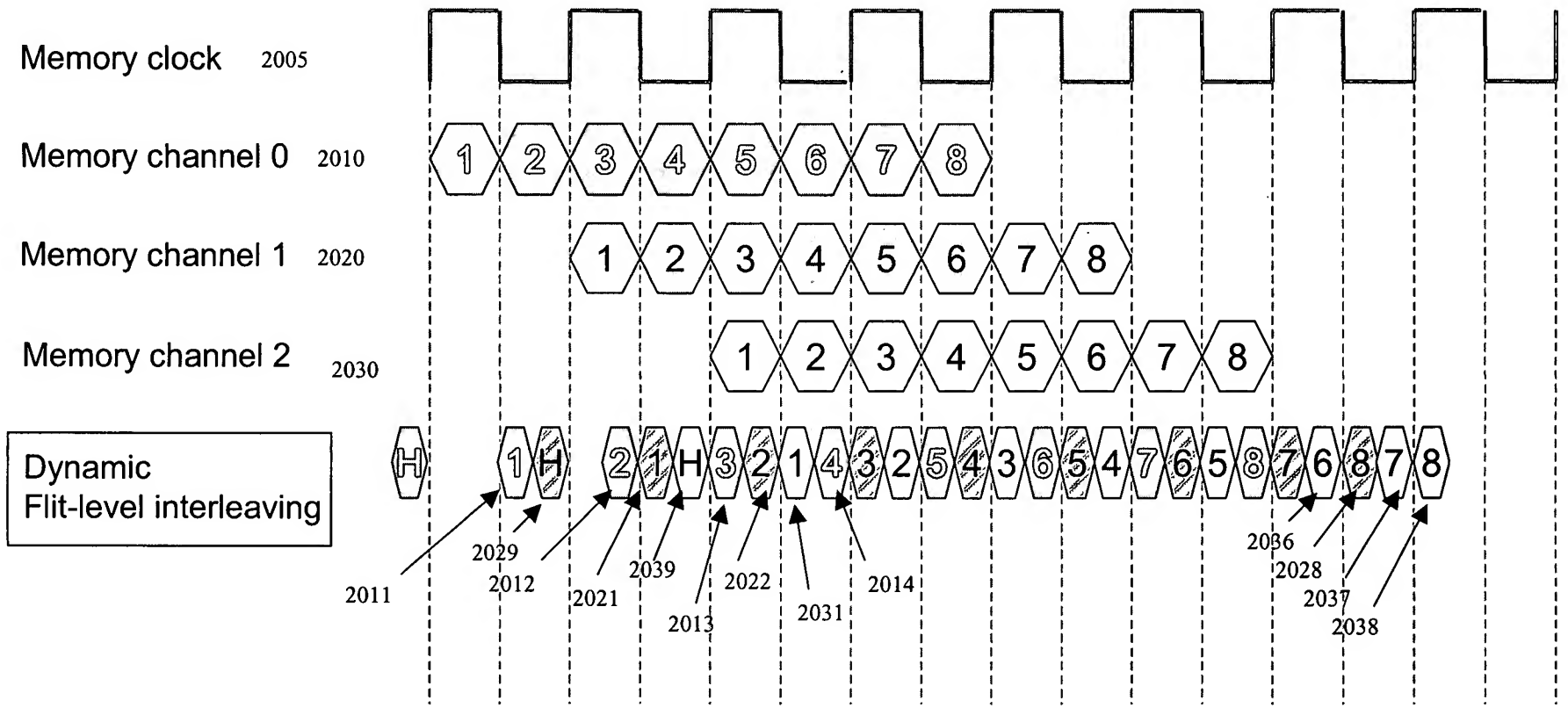
Read return by flit-level interleaving in a 3-memory channel system
Flit clock is 3x of memory clock

Figure 6B



Read return by flit-level interleaving in a 3-memory channel system
Flit clock is 2x of memory clock

Figure 6C



Read return by flit-level interleaving in a 3-memory channel system
Flit clock is 2x of memory clock

Figure 6D